

FIG. 1

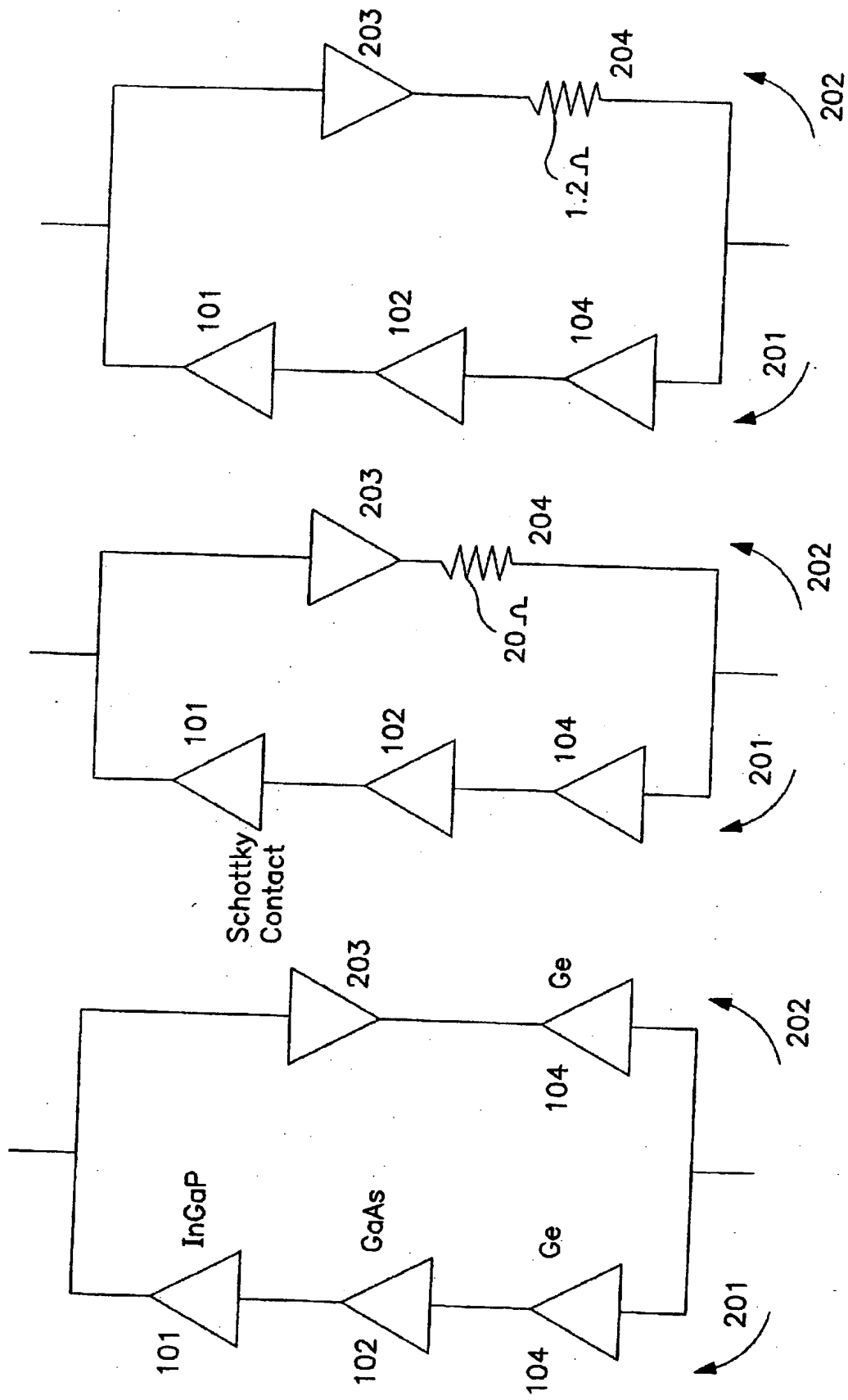


FIG. 2A

FIG. 2B

FIG. 2C

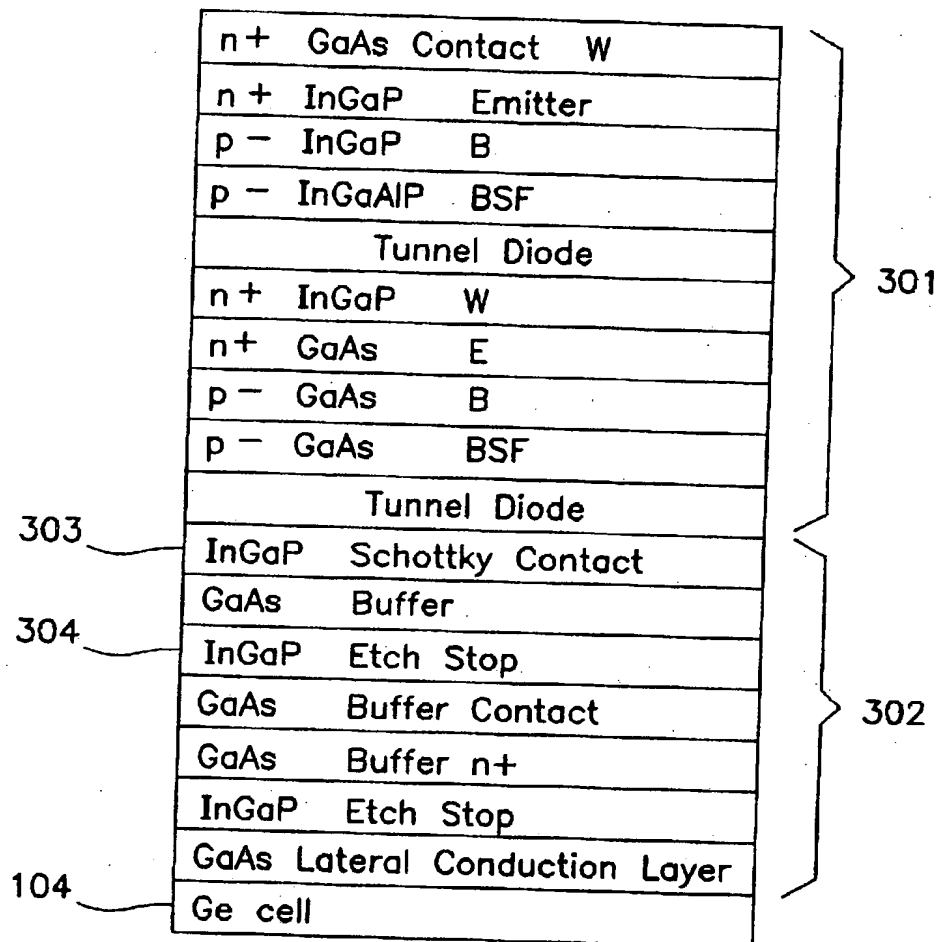


FIG. 3

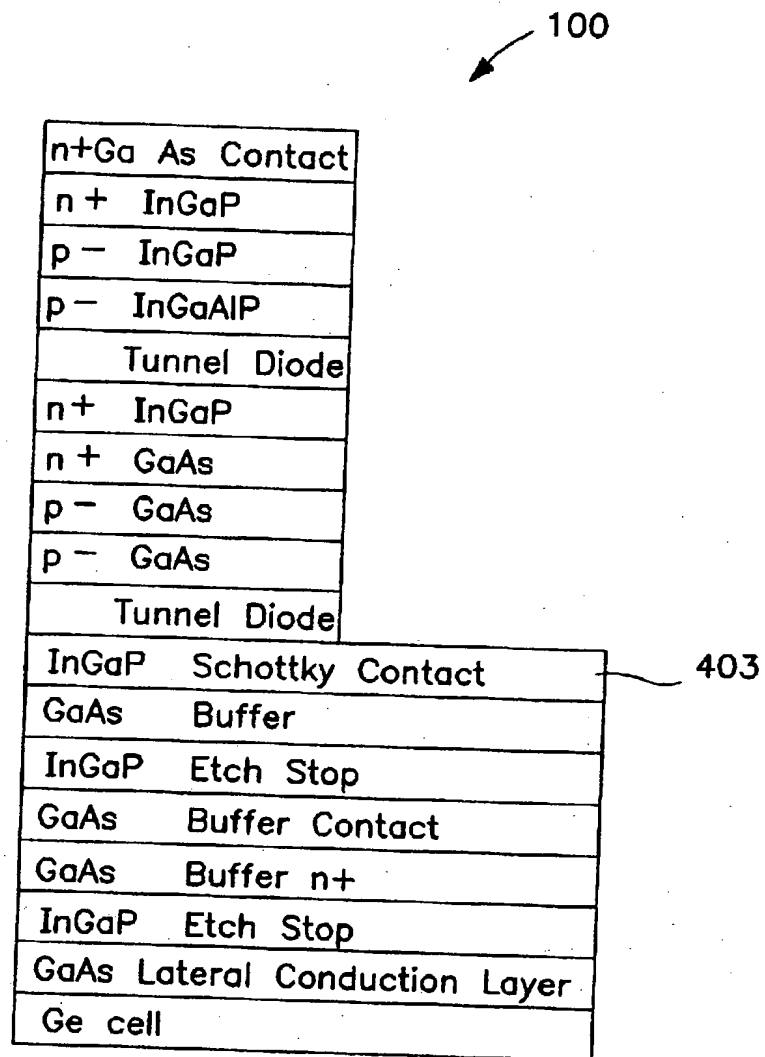


FIG. 4

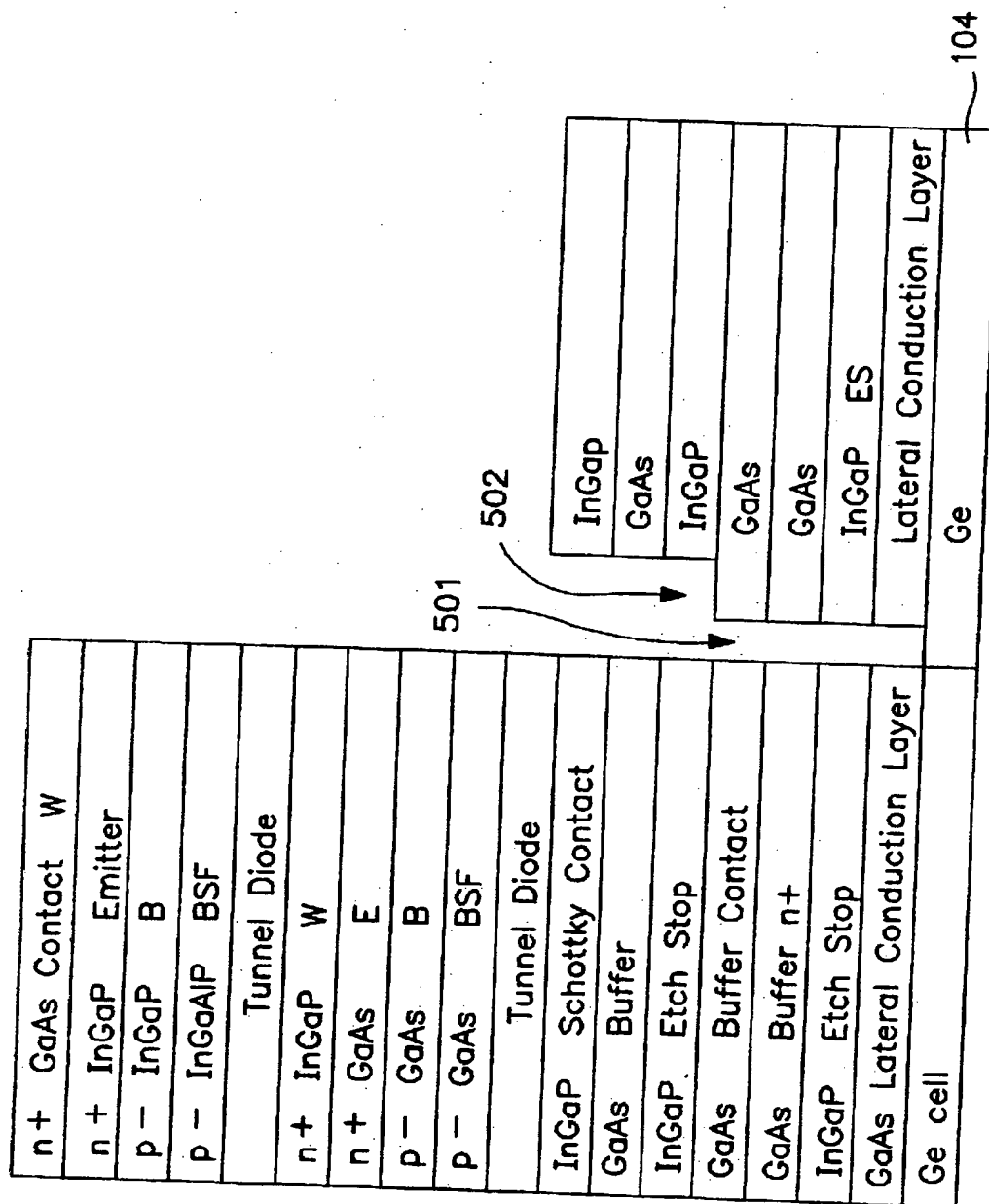


FIG. 5

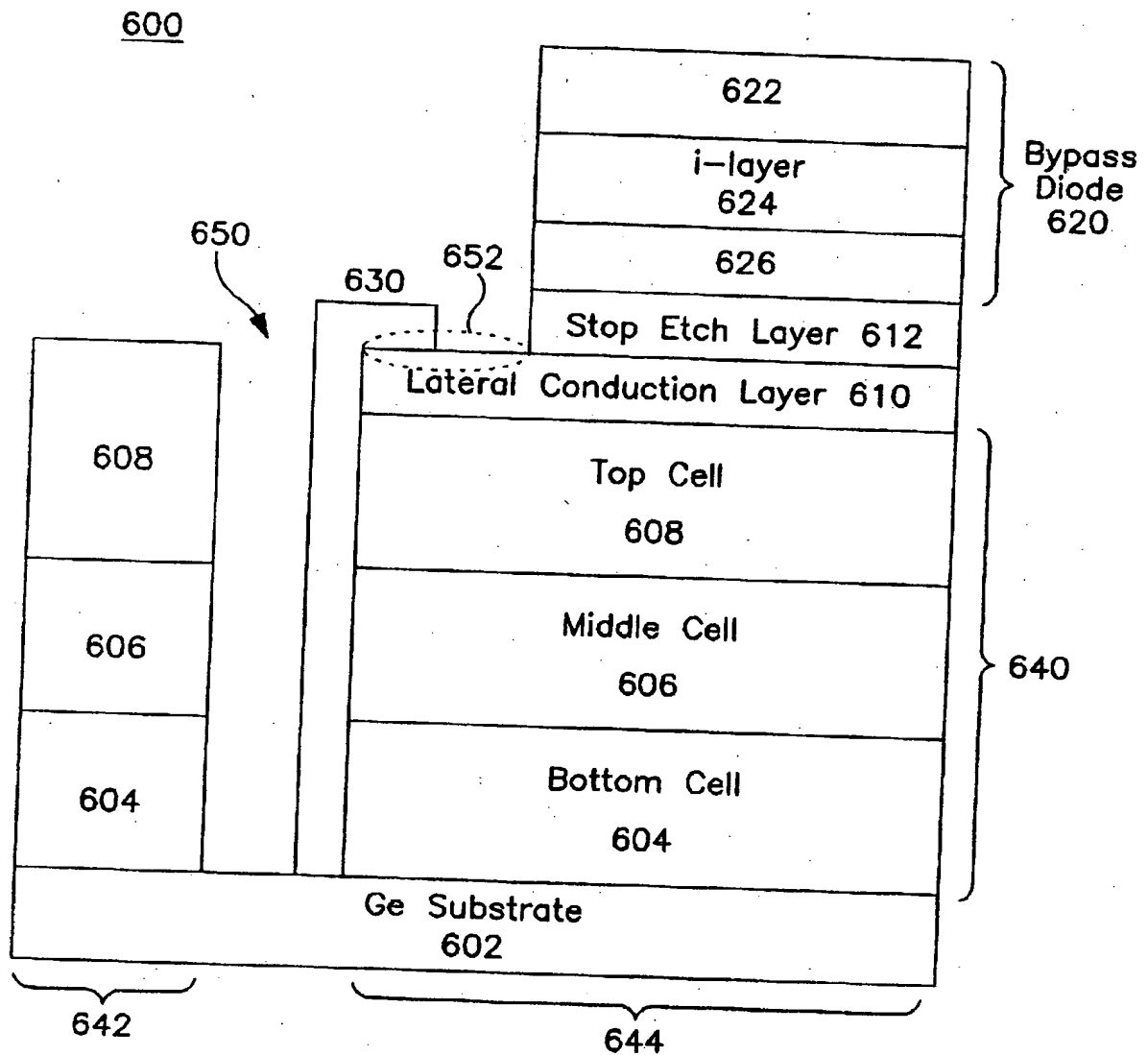


FIG. 6

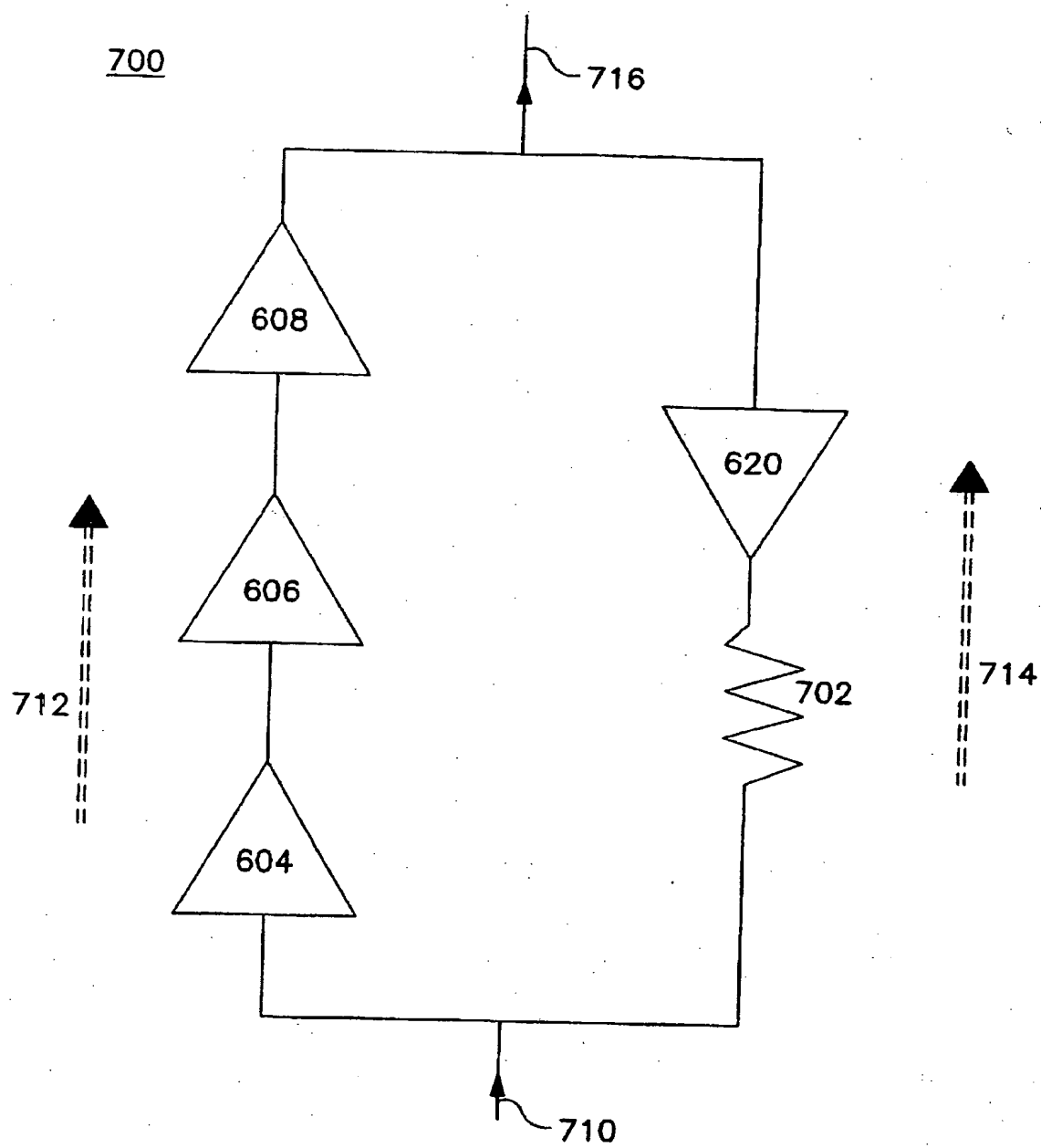


FIG. 7

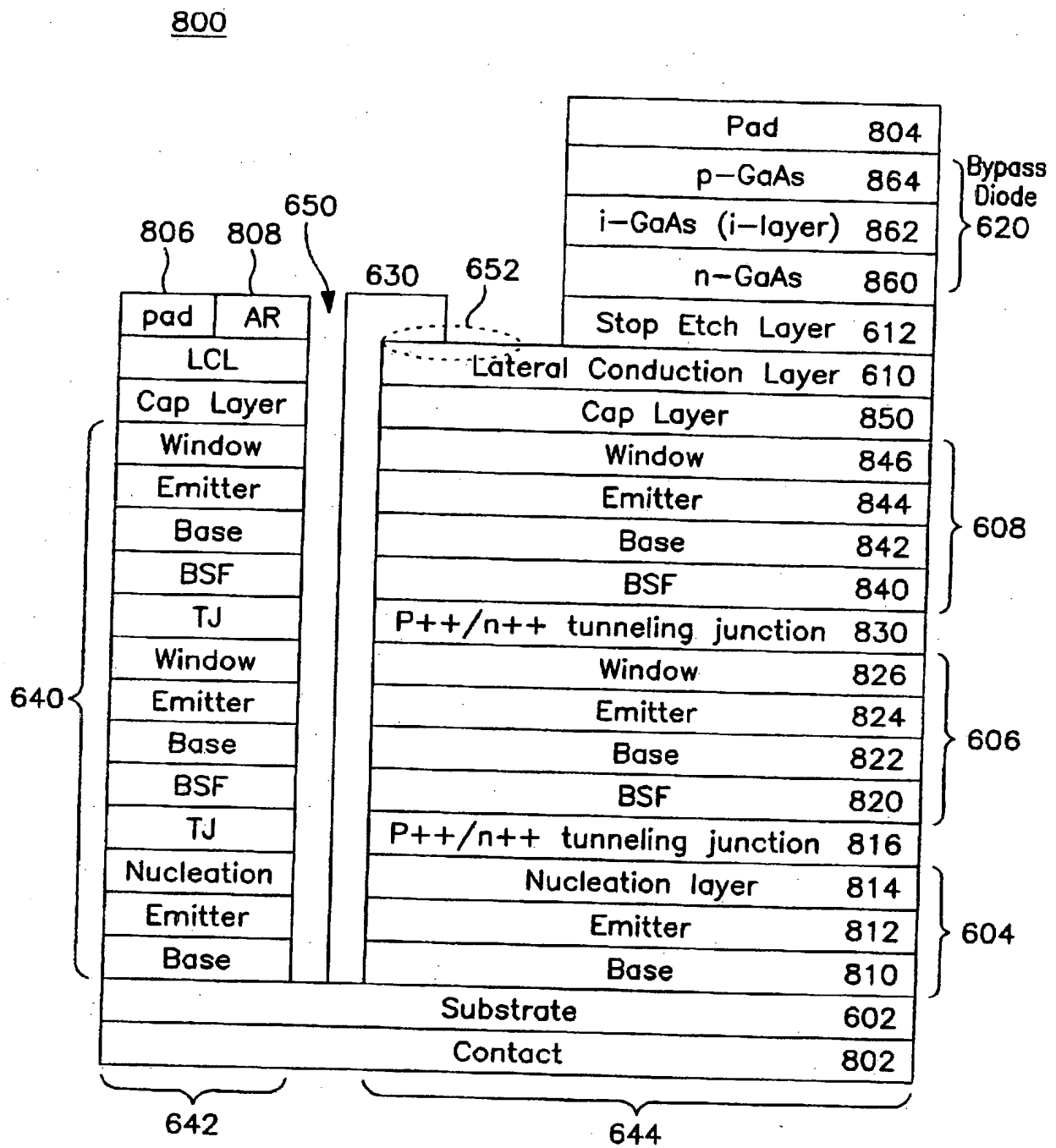


FIG. 8



900

Pad	804	} Bypass Diode 620
p-GaAs	864	
i-GaAs (i-layer)	862	
n-GaAs	860	
Stop Etch Layer	612	} 608
Lateral Conduction Layer	610	
Cap Layer	850	
Window	846	
Emitter	844	
Base	842	
BSF	840	} 606
P++/n++ tunneling junction	830	
Window	826	
Emitter	824	
Base	822	
BSF	820	} 604
P++/n++ tunneling junction	816	
Nucleation layer	814	
Emitter	812	
Base	810	
Substrate	602	
Contact	802	

FIG. 9A

920

922  
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Pad	804	
p-GaAs	864	} Bypass Diode 620
i-GaAs (i-layer)	862	
n-GaAs	860	
Stop Etch Layer	612	
Lateral Conduction Layer	610	
Cap Layer	850	
Window	846	} 608
Emitter	844	
Base	842	
BSF	840	
P++/n++ tunneling junction	830	
Window	826	} 606
Emitter	824	
Base	822	
BSF	820	
P++/n++ tunneling junction	816	} 604
Nucleation layer	814	
Emitter	812	
Base	810	
Substrate	602	
Contact	802	

FIG. 9B

930

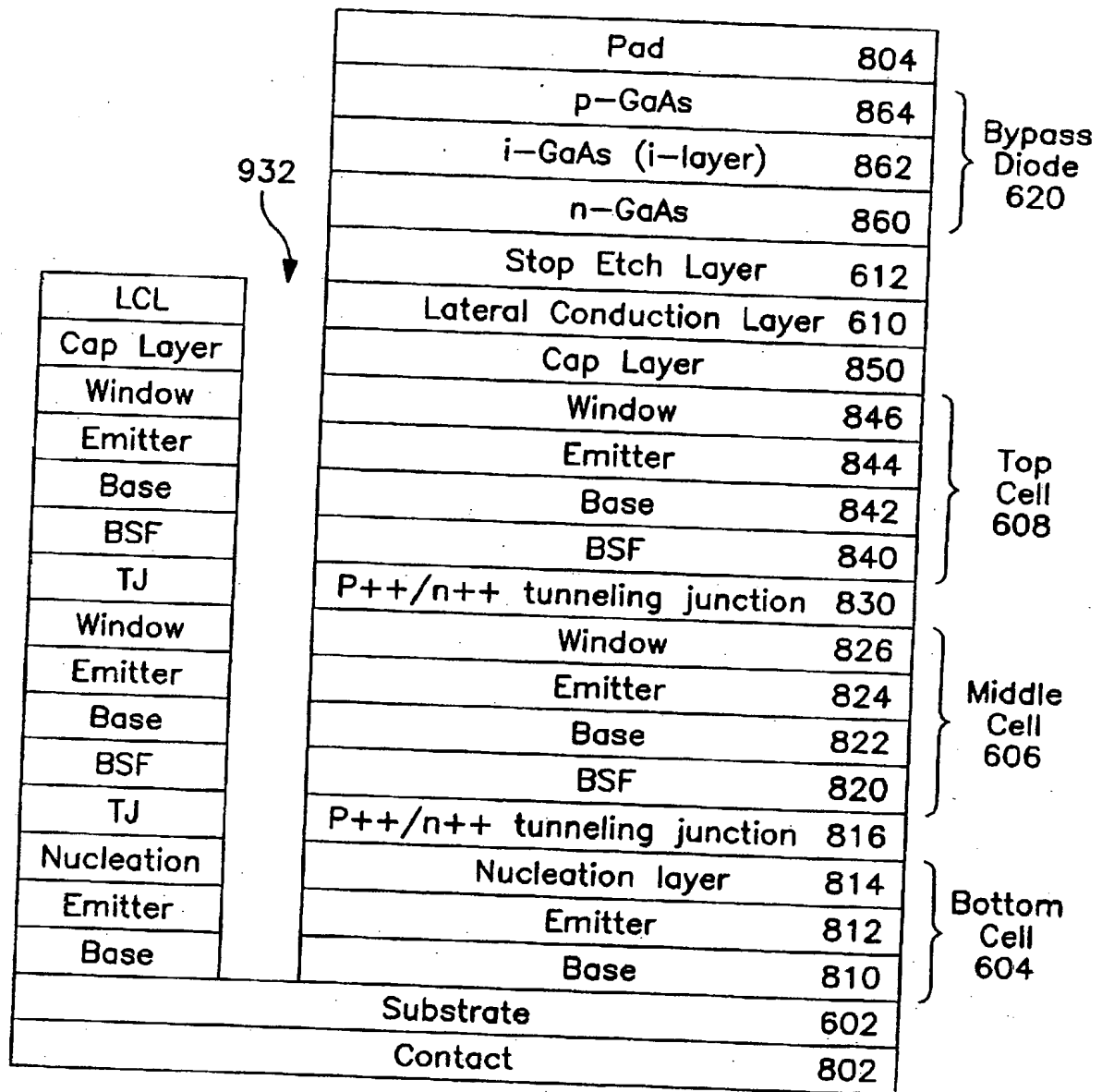


FIG. 9C

940

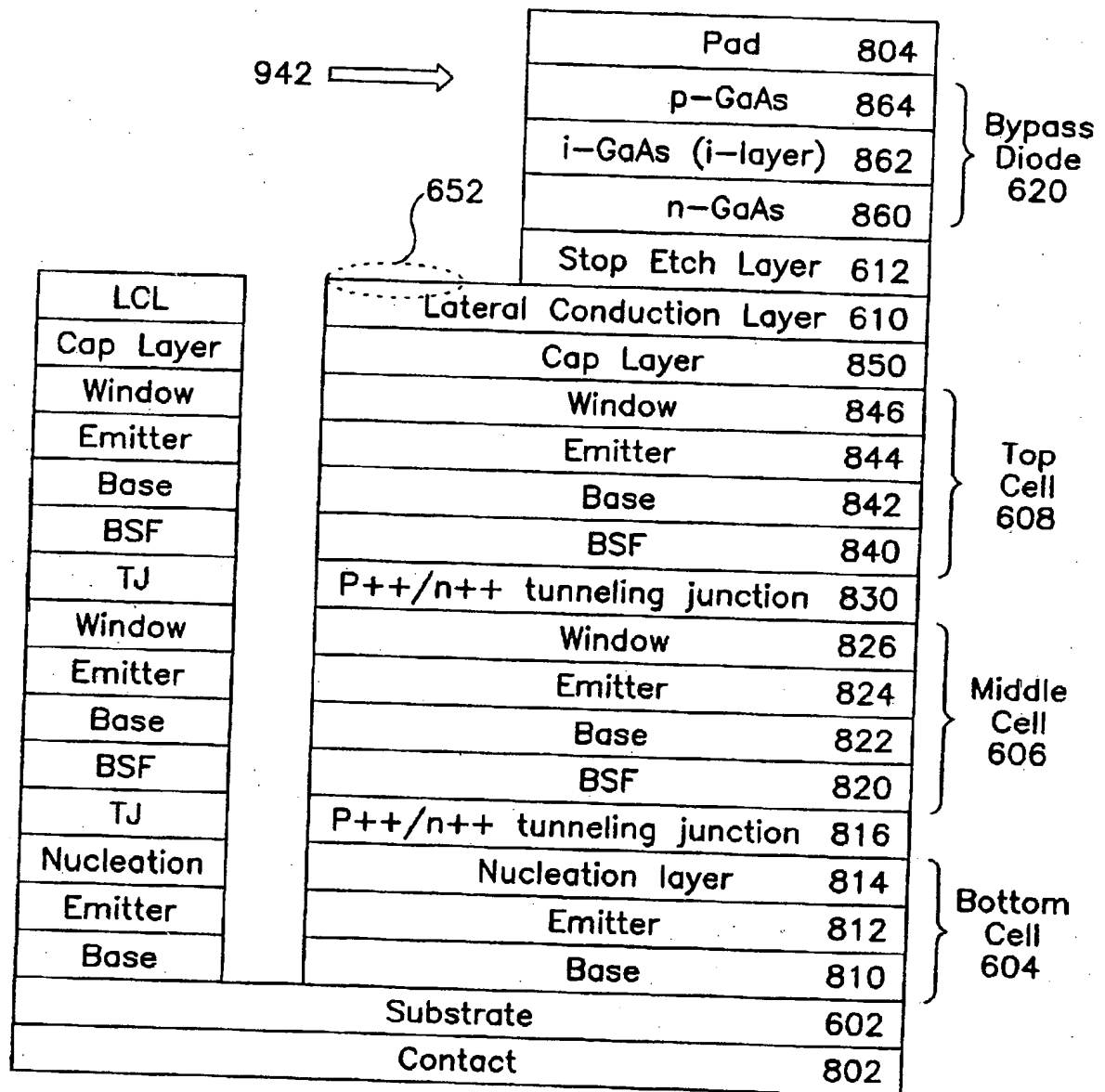


FIG. 9D

950

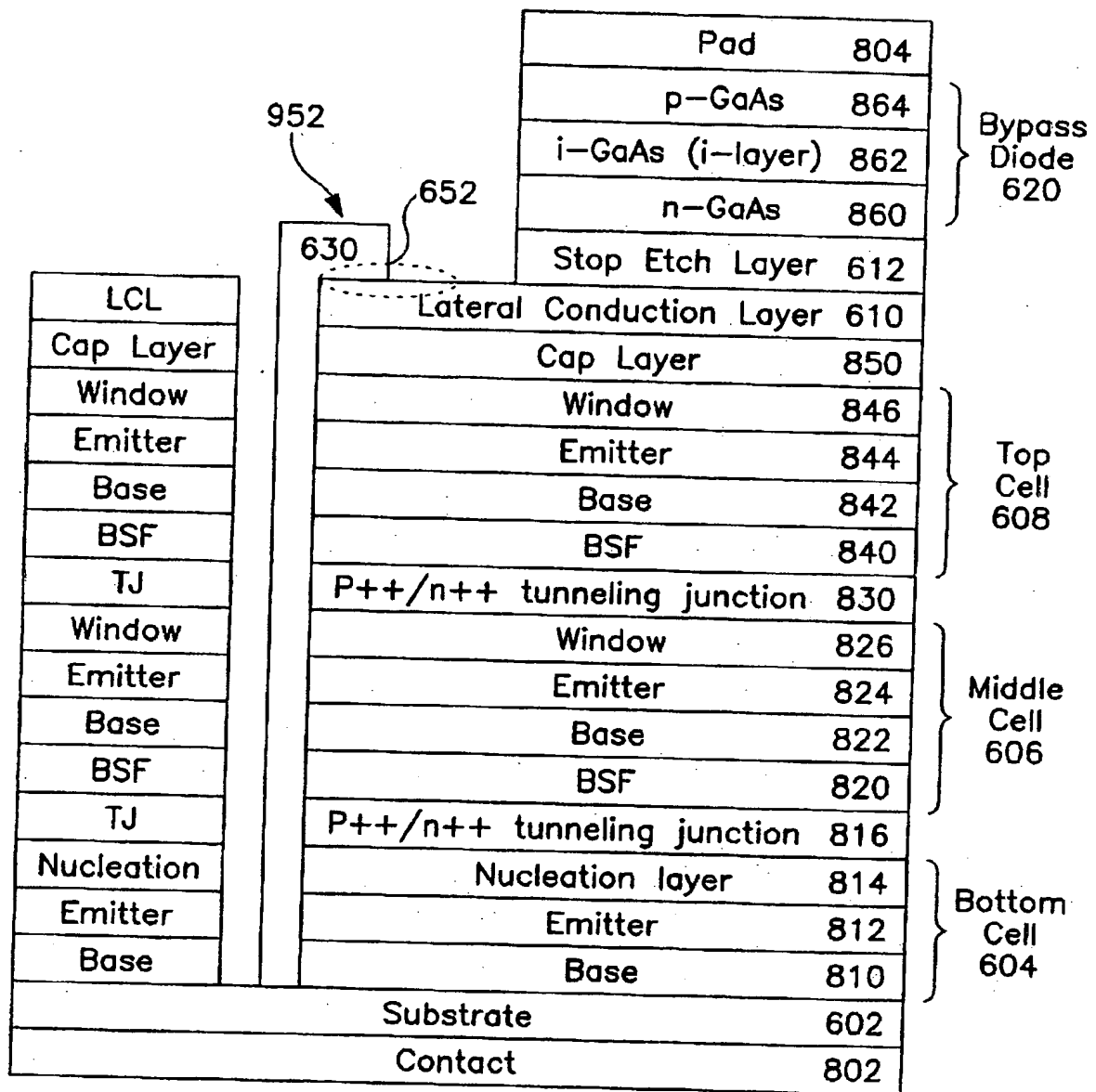


FIG. 9E

1000

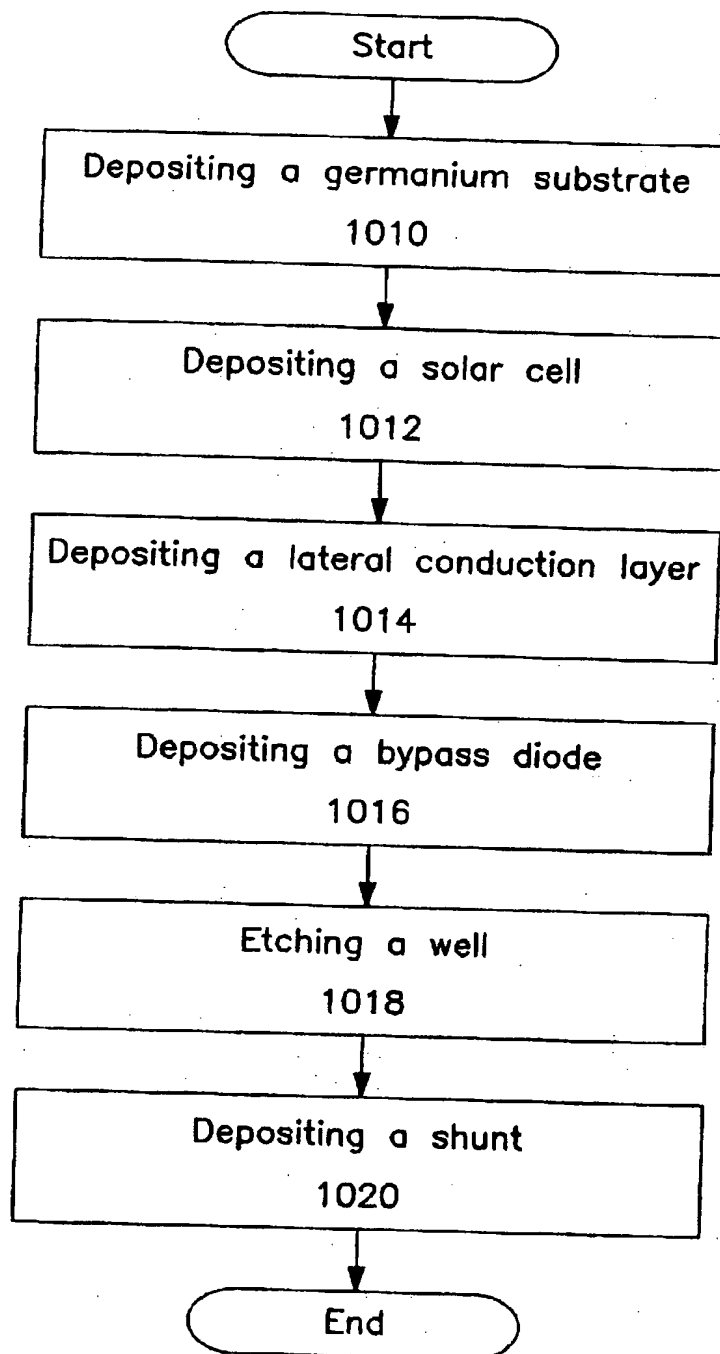


FIG. 10